

09/899,413

"gate inverse clk output" means that the output is the inverse of the clock seen on the gate; and
"Cload" is an expression for capacitance load.

IN THE CLAIMS:

Please substitute the following claims for the same numbered claims in the application.

1 7. (Amended) The method in claim 2, wherein said modifying prevents a delay in
2 propagation of said gating signals across said gating device from inappropriately outputting a
3 portion of a clock pulse.

1 10. (Amended) The method of claim 4, wherein the computing of said setup test comprises:
2 computing a propagated mode test value,
3 computing an input-to-input test value of zero, and
4 using the less pessimistic of said computed test values.

1 14. (Amended) The method in claim 11, wherein said modifying prevents a delay in
2 propagation of said gating signals across said gating device from inappropriately outputting a
3 portion of said clock pulse.

1 21. (Amended) The program storage device in claim 18, wherein said modifying prevents a
2 delay in propagation of said gating signals across said gating device from inappropriately
3 outputting a portion of a clock pulse.